35 USC 102(b) as being anticipated by U.S. Patent No. 5, 821,778 to Bosshart; claims 3-10 were rejected under 35 USC 102(e) as being anticipated by U.S. Patent No. 6,208,170 to Iwaki et al.; claims 14-16 were objected to as being depended upon a rejected base claim, but were indicated as being allowable if rewritten in independent form; and claims 11-13 and 17 were indicated as being allowable.

First, applicants acknowledge with appreciation the indication that claims 11-13 and 17 are allowable and that claims 14-16 would be allowable if rewritten in independent form. By way of this amendment, claims 14-16 have been rewritten in independent form and presently include all the limitations of their respective base claims. Consequently, claims 14-16 are believed to be in condition for allowance.

In response to the objection to the drawings, submitted herewith is a separate letter requesting approval for drawing changes. Figures 2, 9, and 10 will be changed to designate them as "prior art." No further objection on this basis is therefore anticipated.

In response to the objections to claims 3, 5, 8, and 11 for failing to provide an antecedent basis for the limitation "said first transistor," claims 3, 5, 8, and 11 have been rewritten in order to provide the same. No further objection on this basis is therefore anticipated.

Briefly recapitulating, claim 1 defines that some gate circuits among the plurality of gate circuits are composed of transistors having a high threshold voltage and transistors having a low threshold voltage. Consequently, it is possible to operate some gate circuits at high speed. Furthermore, a logic circuit and a switch circuit are provided in some gate circuits, the second and third transistors in the switching circuit are turned off at the same time, and the logic circuit is cut off from the power supply line, thereby restraining a leak current.

In contradistinction thereto, Bosshart illustrates in Fig. 1 logic circuit 20 and transistors 12 and 16. Transistors 12 and 16 are configured to cut off the logic circuit 20 from the power supply line. One of transistors 12 and 16 turns on, and the other turns off the power. Consequently, if the timing of the transistors 12 and 16 deviates, there is a likelihood that a leak current will flow through the power supply line. On the other hand, because the present invention (Claim 1) turns off the second and third transistors at the same time, the leak current does not flow through the power supply line when the gate circuit is in the standby state. Consequently, the subject matter defined by Claim 1 is not believed to be anticipated or rendered obvious by Bosshart.

Claim 3 defines that the gate circuit is connected between a virtual voltage line and a first reference voltage line, and a second transistor is connected between the virtual voltage line and a second reference voltage line. Because the gate circuit is directly connected to the first reference voltage line, it is possible to ensure cutting off the leak path when the second transistor is turned off.

In contradistinction thereto, the circuit of Fig. 4 of Iwaki et al. connects in series the gate circuit 301 and the transistor 105 between the virtual voltage line QVCC and the ground line VSS. Thus, Iwaki et al. neither discloses nor suggests the configuration of directly connecting the gate circuit to the first reference voltage. Consequently, Iwaki et al. is not believed to anticipate or render obvious the subject matter defined by claim 3.

Claim 5 defines that the gate circuit is connected between a first reference voltage line and a virtual voltage line, and a second transistor is connected between the virtual voltage line and a second reference voltage line. Because the gate circuit is directly connected to the first reference voltage line, it is possible to ensure cutting off the leak path when the second transistor is turned off.

In contradistinction thereto, the circuit of Fig. 7 of Iwaki et al. illustrates a transistor 104 and a gate circuit 101 connected in series between the power supply line VCC and the virtual voltage line QVSS. Hence, Iwaki et al. neither discloses nor suggests the configuration of directly connecting the gate circuit to the reference voltage line. Consequently, Iwaki et al. is not believed to anticipate or render obvious the subject matter defined by claim 5.

Claim 8 defines that the threshold voltages of all the transistors in the storage circuit are set higher than that of a first transistor, thereby reducing the power consumption.

In contradistinction thereto, the circuit of Fig. 2 of Iwaki et al. arranges the data storage circuit 303 at the rear stage side of the logic circuit 301. The data storage circuit 303 includes an inverter gate 317 having a low threshold value and inverter gates 316 and 318 having a high threshold value. Applicants respectfully submit that the reason why the data storage circuit 303 of Iwaki et al. has the inverter gate 317 having a low threshold value and the inverter gate 318 having a high threshold value is because the output of the data storage circuit 303 is the last output signal and it is necessary to operate the data storage circuit 303 at high speed. Claim 8 defines outputting the last output signal from the gate circuit. Because it is unnecessary to operate the storage circuit at high speed, claim 8 sets high the threshold voltage of all the transistors in the storage circuit. Thus, Iwaki et al. neither discloses nor suggests the configuration corresponding to the storage circuit of claim 8. Hence, Iwaki et al. is not believed to anticipate or render obvious the subject matter defined by claim 8.

In light of the above discussion, it is respectfully submitted that claims 1, 3, 5, and 8 are patentably distinguishable from the applied patents, and the dependent claims thereof are therefore also patentably distinguishable from the applied patents.

Consequently, in view of the present amendment, no further issues are believed to be outstanding in the present application, and the present application is believed to be in condition for formal allowance. An early and favorable action is therefore respectfully requested.

Respectfully submitted,
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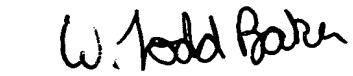

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IN THE CLAIMS

Please amend claims 1, 3, 5, 8, 9, 11, and 14-16 as follows:

1. (Amended) A semiconductor integrated circuit comprising:

a plurality of gate circuits; and

a control circuit configured to control the operation of some gate circuits among said plurality of gate circuits,

each of said some gate circuits among said plurality of gate circuits including:

a logic circuit constituted by a plurality of first transistors; and

a switch circuit which [can switch whether a power supply voltage is supplied to said logic circuit, is constituted by a second transistor having a threshold voltage higher than that of said first transistor, and is controlled by said control circuit] includes second and third transistors controlled to turn on/off by said control circuit, each having a threshold voltage higher than that of each of said first transistors and conductive types different from each other, said switch circuit being capable of cut off said logic circuit from a power supply line by simultaneously turning off said second and third transistors.

3. (Amended) A logic operation circuit comprising:

a gate circuit which is connected between a virtual voltage line and a first reference voltage line and constituted by a plurality of first transistors; and

a second transistor which is connected between a second reference voltage line and said virtual voltage line and constituted by a transistor having a threshold voltage higher than that of each of said first transistors,

a source/drain terminal of each of said first transistors in said gate circuit being connected to either a source/drain terminal of another first transistor in said gate circuit or an output terminal of said gate circuit.

5. (Amended) A logic operation circuit comprising:

a gate circuit which is connected between a first reference voltage line and a virtual voltage line and constituted by a plurality of first transistors;

a second transistor which is connected between said virtual voltage line and a second reference voltage line and has a threshold voltage higher than that of each of said first transistors; and

a third transistor which is connected between said first reference voltage line and an output terminal of said gate circuit and has a threshold voltage higher than that of each of said first transistors,

said second and third transistors being on/off-controlled in such a manner that one of them is turned on while the other is turned off and vice versa.

8. (Amended) A logic operation circuit comprising:

a gate circuit which is constituted by a plurality of first transistors and connected to first and second virtual voltage lines;

a second transistor which is connected between a first reference voltage line and said first virtual voltage line and has a threshold voltage higher than each of said first transistors;

a third transistor which is connected between a second reference voltage line and said second virtual voltage line and has a threshold voltage higher than that of each of said first transistors; and

a storage circuit capable of holding output logic of said gate circuit, said storage circuit being composed of transistors having threshold voltages higher than that of each of said first transistors,

said second and third transistors being controlled to be OFF when said storage circuit holds said output logic of said gate circuit, and said second and third transistors being controlled to be ON when said storage circuit does not hold said output logic of said gate circuit.

9. (Amended) The logic operation circuit according to claim 8, wherein a source/drain terminal of said first transistor in said gate circuit is connected to [either] a source/drain terminal of another first transistor in said gate, to said second reference voltage line circuit or an output terminal of said gate circuit.

11. (Amended) A logic operation circuit comprising:

a gate circuit which is constituted by a plurality of first transistors and connected to first and second virtual voltage lines;

a second transistor which is connected between a first reference voltage line and said first virtual voltage line and has a threshold voltage higher than that of each of said first transistors;

a third transistor which is connected between a second reference voltage line and said second virtual voltage line and has a threshold voltage higher than that of each of said first transistors; and

a bypass circuit which is connected to said gate circuit in parallel and constituted by a circuit substantially equal to said gate circuit by using a plurality of fourth transistors having a threshold voltage higher than that of each of said first transistors,

said bypass circuit being connected between said first and second reference voltage lines.

14. (Amended) A flip flop comprising:

a first conduction interception circuit capable of switching conduction or shutoff between an input terminal and an output terminal;

a first storage circuit capable of holding output logic of said first conduction interception circuit;

a second conduction interception circuit which is capable of switching conduction or shutoff between an input terminal and an output terminal, and has said input terminal being connected to an output terminal of said first storage circuit; and

a second storage circuit capable of holding output logic of said second conduction interception circuit,

said first and second conduction interception circuits [being constituted by said logic operation circuits defined in claim 3,] includes:

a gate circuit which is connected between a virtual voltage line and a first reference voltage line and constituted by a plurality of first transistors; and

a second transistor which is connected between a second reference voltage line and said virtual voltage line and constituted by a transistor having a threshold voltage higher than that of each of said first transistors.

a source/drain terminal of each of said first transistors in said gate circuit being connected to either a source/drain terminal of another first transistor in said gate circuit or an output terminal of said gate circuit, and

said first and second storage circuits being constituted by transistors having a threshold voltage higher than those of said gate circuits in said first and second conduction interception circuits.

15. (Amended) A flip flop comprising:

a first conduction interception circuit capable of switching conduction or shutoff between an input terminal and an output terminal;

a first storage circuit capable of holding output logic of said first conduction interception circuit;

a second conduction interception circuit which is capable of switching conduction or shutoff between an input terminal and an output terminal and has said input terminal being connected to an output terminal of said first storage circuit; and

a second storage circuit capable of holding output logic of said second conduction interception circuit,

said first and second conduction interception circuits [being constituted by said logic operation circuits defined in claim 5,] includes:

a gate circuit which is connected between a first reference voltage line and a virtual voltage line and constituted by a plurality of first transistors;

a second transistor which is connected between said virtual voltage line and a second reference voltage line and has a threshold voltage higher than that of each of said first transistors; and

a third transistor which is connected between said first reference voltage line and an output terminal of said gate circuit and has a threshold voltage higher than that of each of said first transistors,

said second and third transistors being on/off-controlled in such a manner that one of them is turned on while the other is turned off and vice versa, and

said first and second storage circuits being constituted by transistors having a threshold voltage higher than those of said gate circuits in said first and second conduction interception circuits.

16. (Amended) A flip flop comprising:

a first conduction interception circuit capable of switching conduction or interception between an input terminal and an output terminal;

a first storage circuit capable of holding output logic of said first conduction interception circuit;

a second conduction interception circuit which is capable of switching conduction or interception between an input terminal and an output terminal and has said input terminal being connected to an output terminal of said first storage circuit;

and a second storage circuit capable of holding output logic of said second conduction interception circuit,

said first and second conduction interception circuits [being constituted by said logic operation circuits defined in claim 8,] includes:

a gate circuit which is constituted by a plurality of first transistors and connected to first and second virtual voltage lines;

a second transistor which is connected between a first reference voltage line and said first virtual voltage line and has a threshold voltage higher than each of said first transistors;

a third transistor which is connected between a second reference voltage line and said second virtual voltage line and has a threshold voltage higher than that of each of said first transistors; and

a storage circuit capable of holding output logic of said gate circuit, said storage circuit being composed of transistors having threshold voltage higher than that of said first transistor,

said second and third transistors being controlled to be OFF when said storage circuit holds said output logic of said gate circuit, and said second and third transistors being controlled to be ON when said storage circuit does not hold said output logic of said gate circuit, and

said first and second storage circuits being constituted by transistors having a threshold voltage higher than those of said gate circuits in said first and second conduction interception circuits.